Design and Implementation of a Modified FIR Filter Incorporating a Low Power and Area Efficient Carry Select Adder Topology

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***Abstract*—Adders are one of the widely used digital component in digital integrated circuit design. Addition is the heart of computer arithmetic, and arithmetic unit is often the work horse of a computational circuit. They are the necessary components of a data path. Recently, fast adders are used in various applications. Ripple carry adder(RCA) has the most compact design but takes longer computing time. Carry look ahead adder(CLA) gives fast results but consumes large area. Carry select adder(CSLA) is one of the fastest adder used in many data processing applications. It provide a compromise between small area but longer delay RCA and large area with shorter delay CLA. CSLA is used to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. But it is not area efficient, so a gate-level modification is used. This work uses a binary to excess-1 converter(BEC) instead of RCA with Cin =1 to achieve lower area and power consumption. Greater advantage of BEC logic comes from lesser no: of logic gates than a n-bit full adder structure. The proposed work is to implement modified CSLA in digital filters(FIR) for arithmetic and logical operations. Conventional FIR systems has some delay and area problems. It can be reduced by placing modified CSLA as adder component. Also in this paper, a 128-bit modified CSLA is designed and simulated.**

***IndexTerms*—BEC logic,CSLA,FIR filter, RCA, SQRT CSLA.**

INTRODUCTION

Addition is a fundamental and most commonly used arithmetic operation for any digital system, digital signal processing or control system. It is the most often speed limiting element too. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.This makes them suitable and compact VLSI implementations.There are many ways to design an adder. The Ripple Carry Adder provides the most compact design but takes longer computing time. If there is N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the RCA gives highest delay of all adders. The Carry Look Ahead Adder gives fast results but consumes large area. If there is N-bit adder, CLA is fast for N≤4, but for large values of N its delay increases more than other adders. So for higher number of bits, CLA gives higher delay than other adders due to presence of large number of fan-in and a large number of logic gates. The Carry Select Adder (CSA) provides a compromise between small area but longer delay RCA and a large area with shorter delay CLA.. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Among various adders, the CSA is intermediate regarding speed and area . Here Modified Carry Select-Adder (MCSA) architecture to reduce area and power with minimum speed penalty .The MCSA is designed by using single RCA and Binary to Excess-1 Converter instead of using dual Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit positioning an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagate din to the next position. CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders to generate partial sum and carry by considering carry input cin = 0,cin =1and, then the final sum and carry are selected by the multiplexers.The basic idea of this work is to use Binary to Excess-1 Converter instead of RCA with cin=I in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

Then this low power and area efficient carry select is implemented on to a digital FIR filter. The main disadvantage of FIR filters is that considerably more computation power in a general purpose processor is required compared to an IIR filter with similar sharpness or selectivity, especially when low frequency cutoffs are needed. Inorder to make an improvement in the power consumption, the adder section of this conventional FIR filter is replaced by the modified carry select adder. By placing modified carry selectadder, both the power, delay and area can be reduced. Thus the drawback of

FIR filter can be reduced to a much extent. Also modified 128-bit CSLA is designed and simulated.

II. Delay and Area Evaluation Methodology of the BasicAdder Blocks

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig.1.The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter,each having delay equal to 1 unit and area equal to 1 unit. Then add up the number of gates in the longest path of a logic block that contributes to the maximum delay.The area evaluation is done by counting the total number of AOI gates required for each logic block.Based on this approach, the CSLA adder blocks of 2:1mux, Half Adder (HA), and FA are evaluated.

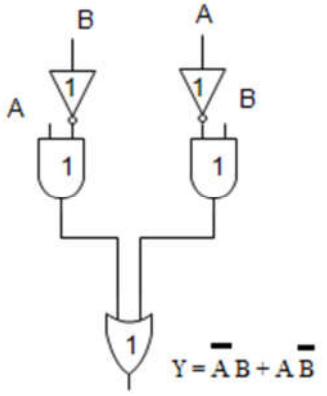

*Fig 1.*Delay and Area evaluation of an XOR gate.

Table 1: Delay And Area Count Of The Basic Blocks Of CSLA

Adder Blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

III. Carry Select Adder with BEC Logic

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. Fig 2 represents BEC logic

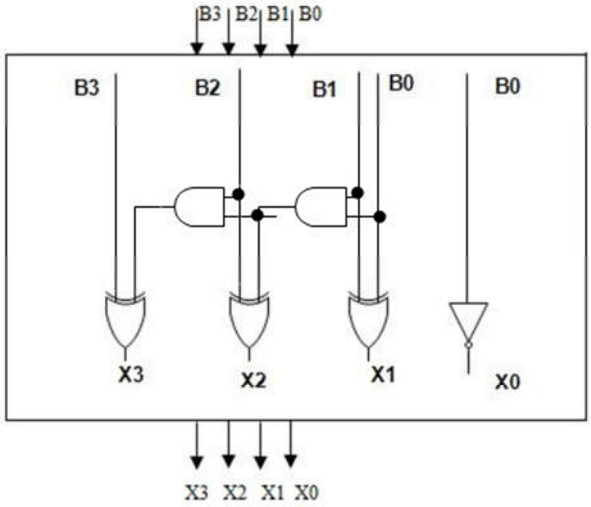

*Fig 2.*4-bit BEC logic.

X0 = ~B0 (1)

X1 = B0^B1 (2)

X2 = B2^(B0 & B1) (3)

X3 = B3^(B0 & B1 & B2) (4)

Above equations represents the expressions for a 4-bit BEC logic.Binary to excess one converter replaces the ripple carry adder for carry input equal to one in the regular square root carry select adder. The main advantage of BEC logic is that it reduces the number of logic gates than the full adder structure. To replace the n bit ripple, carry adder, and n+1 bit BEC is required. Ripple carry adder will produce the sum and carry when carry input equal to zero and BEC will produce the sum and carry when carry input equal to one. Multiplexer will select the required output as per the previous carry output. Since the number of gates in BEC is very much less than that of ripple carry adder.The structure of 16-bSQRT CSLA using BEC for RCA with Cin = 1 is shown in Fig. 3.

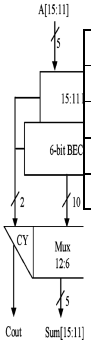

*Fig 3.*16-b Modified carry select adder

The SQRT CSLA using BEC has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively.

IV. FIR FILTER

The advantage of SQRT CSLA using BEC is implemented on to a Digital FIR filter. A finiteimpulseresponse(FIR)filter is a type of a signal processing filter whoseimpulse response (or response to any finite length input) is of *finite* duration, because it settles to zero in finite time. The main disadvantage of FIR filters is that considerably more computation power in a general purpose processor is requiredcomparedtoanIIRfilterwithsimilarsharpnessorselectivity,especiallywhenlowfrequency cutoffs are needed. Also the delay associated with the FIR filter can be much reduced.

In FIR filter, the output y(n) is a function of only past and present inputs.The operation is described by the following equation, which defines the output sequence *y[n]* in terms of its input sequence *x[n]*:

$$y[n] = b_0x[n] + b_1x[n-1] + \cdots + b_Nx[n-N] = \sum_{i=0}^{N} b_ix[n-i] \quad (5)$$

where x[n] is the input signal, y[n] is the output signal, b_i are the filter coefficients, also known as tap weights tha make up the impulse response, N is the filter order,an N th-order filter has $(N+1)$ terms on the right-hand side. The $x[n-i]$ in these terms are commonly referred to as *taps*, based on the structure of a tapped delay linethat in many implementations or block diagrams provides the delayed inputs to the multiplication operations.

The implementation of an FIR requires three basic building blocks multiplication, addition, signal delay. Figure 4 represents the building blocks.

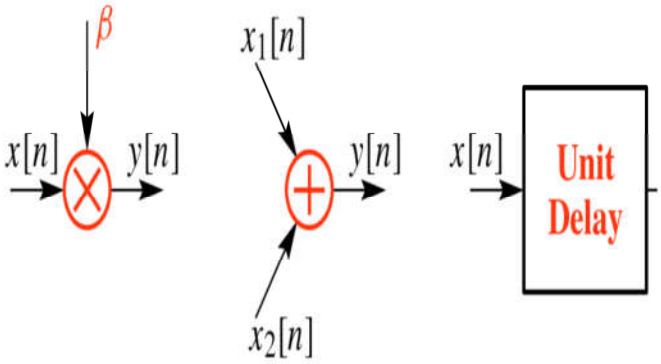

*Fig 4.*Basic building blocks

Multiplier

$$y[n] = \beta\, x[n] \quad (6)$$

In a DSP system the multiplier must be fast and must have sufficient precision (bit width; think logic circuits) to support the desired application. A high quality filter will in general require more multiplications than one of lesser quality, so throughput suffers if the multiplier is not fast.There are classes of filters that do not require multiplies. FIR filters having 50 coefficients or more are not that uncommon

Adder

$$y[n] = x_1[n] + x_2[n] \quad (7)$$

Signal addition is a very basic DSP function. In an FIR filter additions are required in combination with multiplications, hence DSP microprocessors feature multiply-accumulate (MAC) units. Adders generally operate with just two inputs at a time Multiply Add Delay.

Unit Delay

$$y[n] = x[n-1] \quad (8)$$

The unit delay provides a one sample signal delay. A sample value is stored in a memory slot for one sample clock cycle, and then made available as an input to the next processing stage. An *M*-unit delay requires *M* memory cells (note each memory cell must store say *B*-bits) configured as a shift register (*B*-bits wide).

Here the adder component used is modified carry select adder instead of a full adder.

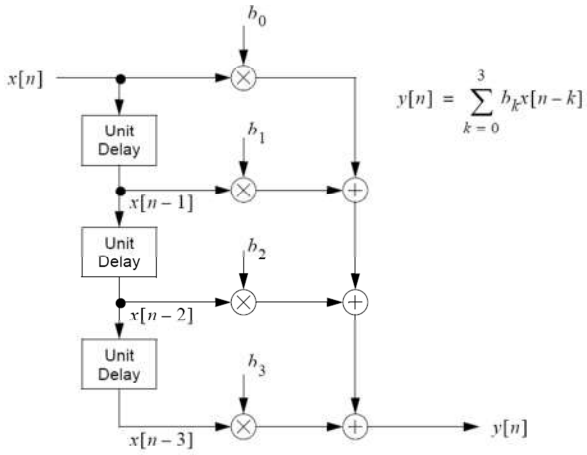

Fig 5. Block diagram of 4-tap filter using modified CSLA

Figure 5. Shows the block diagram of 4-tap filter using modified CSLA. Here the adder component used is

modified carry select adder instead of a normal full adder.Figure 6 indicates adder block in FIR filter.

Fig 6 Adder block in FIR

The impulse response is of finite length *M*, as required. Note that FIR filters have only zeros (no poles). Hence known also as all-zero filters FIR filters also known as feed forward or non-recursive, or transversal.

V. RESULT AND DISCUSSION

The design proposed in this paper has been developed using VHDL and synthesized in Xinx ISE. Figure 7 indicates the simulation result of FIR filter with modified CSLA.X_{in} is the input given to the FIR filter which is 8-bit data. Y_{out} is the output of the FIR filter which is 18-bit. Figure 8 and 9 indicates number of filter slices and number of adder slices respectively for FIR filter with full adder and with modified CSLA.. Figure 10 represents delay comparision.Table 2. indicates comparision table of various parameters.

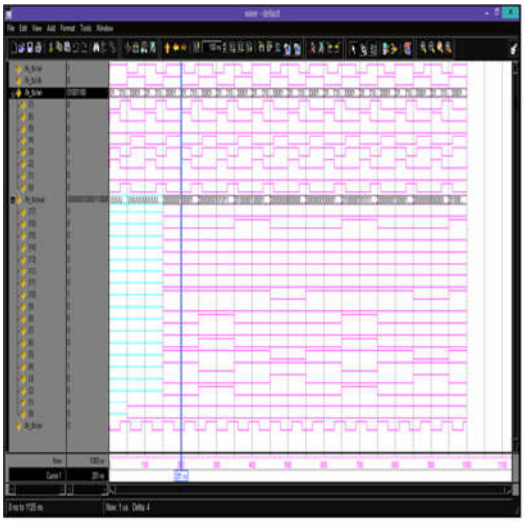

*Fig 7.*Modified carry select adder implemented in FIR

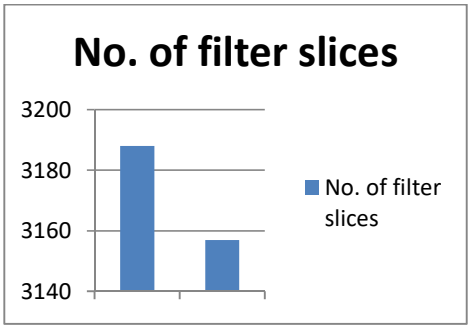

*Fig 8.*Number of filter slices

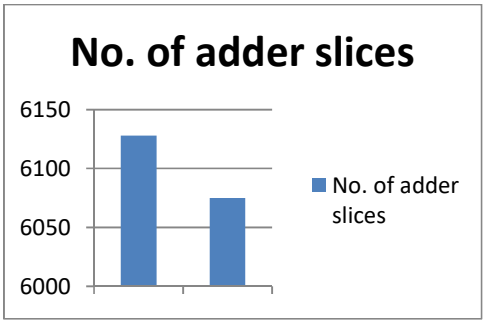

*Fig 9.*Number of adder slices

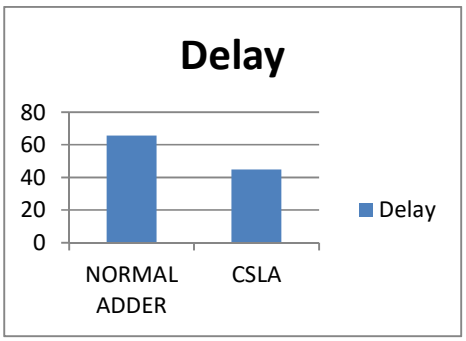

Fig 10.Delay Comparision

Table 2.Comparision table

PARAMETERS	FIR FILTER WITH NORMAL ADDER	FIR FILTER WITH MODIFIED CSLA
Delay(ns)	65.522	44.838
No. of filter slices($nm^{2)}$	3188	3157
No. of adder slices($nm^{2)}$	6128	6075

VI. CONCLUSION

This correspondence has introduced a technique for efficient reduction in delay of digital FIR systems. A systematic design technique is provided and a detailed example shows to addition savings. That is, the adder component in the conventional FIR system is replaced by modified carry select adder. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that normal adder in FIR system has a delay of 65.522 ns, but the modified CSLA has a delay of only 43.838 ns.

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